CLAIMS

What is claimed is:

1. A circuit comprising:

at least one delay element for receiving a signal and for generating a time delay in said signal;

calibration circuit, coupled to said delay element, for calibrating said delay element so as to match said time delay to a predetermined time period; and

multiplier-summing circuit, coupled to said delay element, for multiplying a signal output from said delay element and for summing said multiplied signals to generate an equalized signal.

2. The circuit as set forth in claim 1, wherein:

said calibration circuit comprises a control loop for receiving a reference signal, output from said delay element, and for generating a phase adjustment based on said delay of said reference signal propagated through said delay element; and

said delay element comprises selectable parameters for receiving a phase adjustment from said control loop and for setting said selectable parameters based on said phase adjustment.

3. The circuit as set forth in claim 2, wherein said control loop comprises:

phase detector for measuring a phase difference between said reference signal, input to said delay element, and a signal output from said delay element; and

loop filter, coupled to receive said signal output from said phase detector, for generating said phase adjustment based on a predetermined response of said phase difference.

4. The circuit as set forth in claim 1, wherein:

said calibration circuit comprises:

at least one reference delay element for receiving a reference signal and for generating a delay for said reference signal based on at least one tunable parameter;

control loop, coupled to said reference delay element, for receiving said reference signal, output from said reference delay element, for generating a phase adjustment for said reference delay element based on said delay of said reference signal propagated through said reference delay element, and for tuning said tunable parameter based on said phase adjustment; and

said delay element comprising selectable delay parameters for setting said delay parameters based on said tunable parameter from said reference delay element.

5. The circuit as set forth in claim 1, wherein said delay element comprises a transmission line.

6. The circuit as set forth in claim 5, wherein said delay element further comprises a means for adjusting capacitance for said transmission line, so as to calibrate said delay element.

7. The circuit as set forth in claim 1, wherein said delay element comprises lumped circuit elements .

8. The circuit as set forth in claim 7, wherein said delay element further comprises a means for selecting combinations of said lumped parameters to calibrate said delay element.

9. The circuit as set forth in claim 1, wherein said delay element comprises a plurality of (stub) transmission lines.

10. The circuit as set forth in claim 9, wherein said delay element further comprises a means for selecting a length of said stub transmission lines to calibrate said delay element.

11. A method for filtering a signal, said method comprising the steps of:

receiving a signal in at least one delay element;

generating a time delay in said signal;

calibrating said delay element so as to match said time delay to a predetermined time period;

multiplying a signal output from said delay element; and

summing said multiplied signals to generate an equalized signal.

12. The method as set forth in claim 11, wherein:

the step of calibrating said delay element comprises the steps of receiving a reference signal, output from said delay element, and for generating a phase adjustment based on said delay of said reference signal propagated through said delay element; and

the step of receiving a signal in at least one delay element comprises the steps of receiving a signal in a delay element that comprises selectable parameters, receiving a phase adjustment, and setting said selectable parameters based on said phase adjustment.

13. The method as set forth in claim 12, wherein the step of generating a phase adjustment comprises the steps of:

measuring a phase difference between said reference signal, input to said delay element, and a signal output from said delay element; and

generating said phase adjustment based on a predetermined response of said phase difference.

14. The method as set forth in claim 11, wherein the step of calibrating said delay element comprises the steps of:

receiving a reference signal in at least one reference delay element;

generating a delay for said reference signal based on at least one tunable parameter;

generating a phase adjustment for said reference delay element based on said delay of said reference signal propagated through said reference delay element;

tuning said tunable parameter based on said phase adjustment; and

setting said delay parameters based on said tunable parameter from said reference delay element.

15. The method as set forth in claim 11, wherein said delay element comprises a transmission line.

16. The method as set forth in claim 15, further comprising the steps of adjusting capacitance for said transmission line, so as to calibrate said delay element.

17. The method as set forth in claim 11, wherein said delay element comprises lumped circuit elements .

18. The method as set forth in claim 17, further comprising the step of selecting combinations of said lumped parameters to calibrate said delay element.

19. The method as set forth in claim 11, wherein said delay element comprises a plurality of (stub) transmission lines.

20. The method as set forth in claim 19, further comprising the step of selecting a length of said stub transmission lines to calibrate said delay element.

21. A method for filtering a signal, said method comprising the steps of:

receiving a signal in at least one delay element;

multiplying a signal output in a plurality of multipliers;

generating a time delay in signals output from said multipliers;

calibrating said delay element so as to match said time delay to a predetermined time period;

summing time delayed signals to generate an equalized signal.

22. A circuit comprising:

a plurality of multiplier circuits, coupled in series, for multiplying a signal in each of said multipliers;

a plurality of delay elements for receiving multiplied signals from said multipliers and for generating a time delay in said signal, said delay elements being coupled in series to sum said multiplied signals to generate an equalized signal; and

calibration circuit, coupled to said delay elements, for calibrating said delay elements so as to match said time delays to predetermined time periods.